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| 10/665,293 | 09/22/2003 | Wei-Han Chang | TOP 332 | 5627 |

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|---|---|
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| **ART UNIT** | **PAPER NUMBER** |
| 2114 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/665,293 | CHANG ET AL. | |
| | Examiner | Art Unit | |
| | David G. Gentry | 2114 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

Claim 5 is objected to because of the following informalities: The word "determine" on line 10 should be changed to "determining". Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Line 8 states "determining whether to ignore a reloading function". It is unknown what a reloading function is or what its purpose is at it is not mentioned in the specification. It is given the broadest interpretation possible as any function that aids in the reloading of the system.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-4+12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein (U.S. Patent No. 5,938,764) in view of DMI v2.0 Update.

As per claim 1, Klein discloses a method of backing up BIOS settings stored in a CMOS memory in a computer system by a memory, the method comprising steps of:

executing a power on self test (POST) procedure after powering on the computer system (column 5, lines 6-26, specifically lines 6-9; Note: it is understood that a POST test is simply an initialization test run upon power up of the computer);

detecting BIOS settings stored in the CMOS memory (column 5, lines 20-22; the CMOS RAM configuration data is described in relation to BIOS in column 1, lines 43-49); and

writing predetermined BIOS settings stored in the memory into the CMOS memory if the BIOS settings stored in the CMOS memory are abnormal (column 5, lines 34-38).

DMI memory, a term not commonly used in the art, is defined as being memory that stores information according to DMI standards.

Klein fails to disclose DMI memory.

DMI v2.0 Update discloses DMI memory (page 2, lines 8-13).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the DMI memory as disclosed by the DMI v2.0 Update in the method described by Klein. It would have been obvious because the DMI memory would allow DMI-enabled management applications to access the configuration information described by Klein (DMI v2.0 Update: page 2, lines 14-16).

As per claim 2, Klein discloses a method wherein the computer system subsequently accomplishes the POST procedure if the BIOS settings stored in the CMOS memory are normal (column 5, lines 23-27).

As per claim 3, Klein discloses a method wherein the BIOS settings are backed up in a memory block of the memory (column 4, lines 62-64; It is understood that the configuration ROM must be stored in some type of block).

DMI v2.0 Update discloses DMI memory (page 2, lines 8-13).

As per claim 4, Klein discloses a method wherein the memory is located in a flash memory (column 4, lines 2-7).

DMI v2.0 Update discloses DMI memory (page 2, lines 8-13).

As per claim 12, Klein discloses a method of backing up BIOS settings stored in a CMOS memory in a computer system into a memory, comprising:

entering a BIOS setting menu (figure 2B, items 86, 88, and 90);

querying whether BIOS settings being save after exiting the BIOS setting menu (figure 2B, item 92);

backing up the BIOS settings into the memory (figure 2B, item 94).

DMI memory, a term not commonly used in the art, is defined as being memory that stores information according to DMI standards.

Klein fails to disclose DMI memory.

DMI v2.0 Update discloses DMI memory (page 2, lines 8-13).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the DMI memory as disclosed by the DMI v2.0 Update in the method described by Klein. It would have been obvious because the DMI memory would allow DMI-enabled management applications to access the configuration information described by Klein (DMI v2.0 Update: page 2, lines 14-16).

As per claim 13, Klein discloses a method wherein the BIOS settings are stored in a memory block of the memory (column 4, lines 62-64; It is understood that the configuration ROM must be stored in some type of block).

DMI v2.0 Update discloses DMI memory (page 2, lines 8-13).

As per claim 14, Klein discloses a method wherein the memory is located in a flash memory (column 4, lines 2-7).

DMI v2.0 Update discloses DMI memory (page 2, lines 8-13).

As per claim 15, Klein discloses a method wherein the BIOS settings are not saved if saving BIOS settings after exiting the BIOS settings menu is not required (figure 2B, items 92 and 64).

As per claim 16, Klein discloses a method of backing up a BIOS setting stored in the CMOS memory of a computer system by a DMI memory, the DMI memory including a memory block for storing predetermined BIOS settings in the computer system, the method comprising the following steps:

storing the predetermined BIOS settings stored in the CMOS memory to the memory block of the memory (column 5, line 66- column 6, line 5);

updating the BIOS settings stored in the CMOS memory according to the predetermined BIOS setting stored in the memory block of the memory (column 5, lines 34-38).

DMI memory, a term not commonly used in the art, is defined as being memory that stores information according to DMI standards.

Klein fails to disclose DMI memory.

DMI v2.0 Update discloses DMI memory (page 2, lines 8-13).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the DMI memory as disclosed by the DMI v2.0 Update in the method described by Klein. It would have been obvious because the DMI memory would allow DMI-enabled management applications to access the configuration information described by Klein (DMI v2.0 Update: page 2, lines 14-16).

As per claim 17, Klein discloses a method wherein the corresponding memory block of the memory is located in a flash memory (column 4, lines 2-7).

DMI v2.0 Update discloses DMI memory (page 2, lines 8-13).

Claims 5-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein in view of DMI v2.0 Update in further view of Hasbun et al. (U.S. Patent No. 6,295,619).

As per claim 5, Klein discloses a method of backing up BIOS settings stored in a CMOS memory in a computer system by a DMI memory, the method comprising the steps of:

executing a power on self test (POST) procedure after powering on the computer system (column 5, lines 6-26, specifically lines 6-9; Note: it is understood that a POST test is simply an initialization test run upon power up of the computer);

detecting whether the BIOS settings stored in the CMOS memory are normal (figure 2A, item 66; column 5, lines 20-25);

determining whether to ignore a reloading function (column 5, lines 9-15; Note: the reset vector represents the reloading function);

determining whether to access the DMI memory according to whether an enabling signal has been set (column 5, lines 9-15; Note: the reset vector/ warm start also represents the enabling signal); and

writing predetermined BIOS settings stored in the DMI memory into the CMOS memory (column 5, lines 34-38).

Klein fails to disclose detecting header data of the DMI memory.

Hasbun discloses a computer system comprising:

detecting header data of the DMI memory (column 5, lines 35-43).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the header detection as described by Hasbun in the method described by Klein. It would have been obvious because Hasbun allows for a specific sector needed (i.e. the BIOS settings sector) when the data is to be read (column 5, lines 35-43).

DMI memory, a term not commonly used in the art, is defined as being memory that stores information according to DMI standards.

Klein and Hasbun fail to disclose DMI memory.

DMI v2.0 Update discloses DMI memory (page 2, lines 8-13).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the DMI memory as disclosed by the DMI v2.0 Update in the method described by Klein and Hasbun. It would have been obvious because the DMI memory would allow DMI-enabled management applications to access the configuration information described by Klein (DMI v2.0 Update: page 2, lines 14-16).

As per claim 6, Klein discloses a method wherein the computer system subsequently accomplishes the POST procedure if the BIOS settings stored in the CMOS memory are normal (figure 2A, items 66 and 64).

As per claim 7, Klein discloses a method wherein the computer system subsequently accomplishes the POST procedure if the reloading function is ignored (column 5, lines 6-15).

As per claim 8, Hasbun discloses a method wherein the computer system

subsequently accomplishes the procedure if the memory has no header information (column 9, lines 1-6).

Klein discloses a POST procedure (column 5, lines 6-26, specifically lines 6-9; Note: it is understood that a POST test is simply an initialization test run upon power up of the computer).

DMI v2.0 Update discloses DMI memory (page 2, lines 8-13).

As per claim 9, Klein discloses a method wherein the computer system subsequently accomplishes the POST procedure if the enabling signal is not set (column 5, lines 6-15).

As per claim 10, Klein discloses a method wherein the BIOS settings are backed up in a memory block of a memory (column 4, lines 62-64; It is understood that the configuration ROM must be stored in some type of block).

DMI v2.0 Update discloses DMI memory (page 2, lines 8-13).

As per claim 11, Klein discloses a method wherein the memory is located in a flash memory (column 4, lines 2-7).

DMI v2.0 Update discloses DMI memory (page 2, lines 8-13).

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Klein and DMI v2.0 Update, in further view of Cluff et al. (U.S. Patent No. 5,962,930).

Klein and DMI v2.0 Update are relied upon for reasons stated in the previous section.

Klein fails to disclose the CMOS memory located in a south bridge chipset, although he does disclose a bridge circuit (column 3, lines 43-45).

Cluff discloses a method wherein the CMOS memory is located in a south bridge chipset (column 3, lines 1-6).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the CMOS memory in the south bridge chip as described by Cluff in the computer system described by Klein. It would have been obvious because it is a typical place to locate the CMOS (column 3, lines 1-6), seeing as the south bridge chip only relates to where the chip is drawn in a figure.

Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein in view of DMI v2.0 update, Cluff, Burton (U.S. Patent No. 6,996,656), and James et al. (U.S. Patent No. 6,647,512).

As per claim 19, Klein discloses a computer system for backing up BIOS settings in a memory block of a flash memory, comprising:

a central processing unit (CPU) (column 3, lines 29-33); and

a flash memory located on a motherboard of the computer system (column 3, lines 29-30; Note: it is understood that the computer system in figure 1 is located on some type of motherboard), wherein the flash memory comprises a first memory block for a DMI memory (column 3, line 66- column 4, line 7).

Klein fails to disclose CMOS memory located in the south bridge chip.

Cluff discloses a computer system comprsing:

a CMOS memory located in the south bridge chip (column 3, lines 1-6).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the CMOS memory in the south bridge chip as described by Cluff in the computer system described by Klein. It would have been obvious because it is a typical place to locate the CMOS (column 3, lines 1-6), seeing as the south bridge chip only relates to where the chip is drawn in a figure.

Klein and Cluff fail to disclose an FSB or a DDR memory bus.

Burton discloses a computer system comprsing:

a front side system bus (FSB) for connecting a north bridge chip to the CPU (column 4, lines 4-6); and

a double data rate (DDR) memory bus for connecting the north bridge chip to a memory module (column 4, lines 6-13).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the CMOS memory in the south bridge chip as described by Cluff in the computer system described by Klein and Cluff. It would have been obvious because these are typical bus types used in the art (column 3, lines 62-63).

Klein, Cluff, and Burton fail to disclose an AGP or PCI bus.

James discloses a computer system comprsing:

an accelerated graphic port (AGP) bus for connecting the north bridge chip to a display card module (figure 2, item 208; column 4, lines 22-25); and

a peripheral component interconnect (PCI) bus for connecting a south bridge chip to a plurality of peripheral devices (column 4, lines 25-31; column 4, lines 38-41).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the CMOS memory in the south bridge chip as described by Cluff in the computer system described by Klein, Cluff, and Burton. It would have been obvious because these are well-known bus types used in the art.

DMI memory, a term not commonly used in the art, is defined as being memory that stores information according to DMI standards.

Klein, Cluff, Burton, and James fail to disclose DMI memory.

DMI v2.0 Update discloses DMI memory (page 2, lines 8-13).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the DMI memory as disclosed by the DMI v2.0 Update in the method described by Klein. It would have been obvious because the DMI memory would allow DMI-enabled management applications to access the configuration information described by Klein (DMI v2.0 Update: page 2, lines 14-16).

As per claim 20, Klein discloses a computer system wherein the BIOS settings are stored in the CMOS memory (column 3, lines 60-64).

As per claim 21, Klein discloses a computer system wherein the memory block of the flash memory (column 4, lines 2-7) comprises a memory block for the memory (column 4, lines 62-64; It is understood that the configuration ROM must be stored in some type of block), and the memory backs up the BIOS settings (column 4, lines 36-38).

DMI v2.0 Update discloses DMI memory (page 2, lines 8-13).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David G. Gentry whose telephone number is (571) 272-2570. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER